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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ROBERT E. CYPHER and STEVAN A. VLAOVIC

Appeal 2008-4722
Application 10/821,431[1]
Technology Center 2100

Decided:[2] April 29, 2009

Before JOSEPH L. DIXON, JEAN R. HOMERE, and
CAROLYN D. THOMAS, *Administrative Patent Judges*.

THOMAS, *Administrative Patent Judge*.

DECISION ON APPEAL

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[1] Application filed April 9, 2004. The real party in interest is Sun Microsystems, Inc.

[2] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 CFR § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date.

I. STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134(a) from a final rejection of claims 1-4, 6-11, 13-17, 19-24, 26, and 27 mailed November 9, 2006, which are all the claims remaining in the application, as claims 5, 12, 18, and 25 are cancelled. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

A. INVENTION

Appellants invented a branch prediction mechanism that includes a first storage including a first plurality of locations for storing a first set of partial prediction information. The branch prediction mechanism may also include a second storage including a second plurality of locations for storing a second set of partial prediction information. Further, the branch prediction mechanism may include a control unit that performs hash functions on input branch information to generate indexes for accessing a selected location within storage. (Spec., ¶ [0007].)

B. ILLUSTRATIVE CLAIM

The appeal contains claims 1-4, 6-11, 13-17, 19-24, 26, and 27. Claims 1, 14, and 27 are independent claims. Claim 1 is illustrative:

> 1. A branch prediction mechanism comprising:
>
> a first storage including a first plurality of locations for storing a first set of partial prediction information;

a second storage including a second plurality of locations for storing a second set of partial prediction information; and

a control unit configured to perform a first hash function on input branch information to generate a first index for accessing a selected location within said first storage and to perform a second hash function on said input branch information to generate a second index for accessing a selected location with said second storage, wherein said input branch information includes address information corresponding to a fetch address of a current instruction;

wherein said control unit is further configured to provide a prediction value based on corresponding partial prediction information in said selected locations of said first and said second storages; and

wherein said control unit is further configured to update said selected locations of said first and said second storages dependent on whether said prediction value yields an accurate branch prediction.

C. REFERENCES

The references relied upon by the Examiner in rejecting the claims on appeal are as follows:

McFarling	US 2001/0056531 A1	Dec. 27, 2001
Yeh	US 6,427,206 B1	Jul. 30, 2002
Loh	US 2005/0223203 A1	Oct. 6, 2005 (Filed Mar. 30, 2004)

D. REJECTIONS

The Examiner entered the following rejections which are before us for review:

(1) Claims 1-4, 6-8, 13-17, 19-21, 26, and 27 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Loh in view of McFarling.

(2) Claims 9-11 and 22-24 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Loh and McFarling in view of Yeh.

II. PROSECUTION HISTORY

Appellants appealed from the Final Rejection and filed an Appeal Brief (App. Br.) on May 10, 2007. The Examiner mailed an Examiner's Answer (Ans.) on August 2, 2007. No Reply Brief is found in the record.

III. FINDINGS OF FACT

The following findings of fact (FF) are supported by a preponderance of the evidence.

Loh

1. Loh discloses that "**FIG. 4** illustrates a prediction history register **401**, in which prediction history is stored in one embodiment of the invention. The prediction history register may also be a memory location instead of a register within the processor or some combination thereof" (¶ [0018]).

2. Loh discloses that "some intermediate branch history units may be in parallel and others may be in series with any of the parallel branch history units" (¶ [0019]).

3. Loh discloses "a final branch history predictor unit **410** to generate a final branch prediction as function of the intermediate branch predictions performed by the intermediate branch prediction units" (¶ [0020]).

McFarling

4. McFarling discloses "a predictor, called a global shared index or 'gshare' predictor" (¶ [0026]).

5. McFarling discloses that "[a]s shown in **FIG. 5**, a typical gshare predictor uses the branch instruction address on line **50** XOR'ed with the global history register **52** to index the array of counters **54**. This hashing allows using more history bits and more address bits with the same number of counters, improving global prediction accuracy" (¶ [0026]).

6. McFarling discloses that "[t]he value V^+ provides the basis for making the global stage prediction. V^{30} could be used to directly access an array of counters . . . A better approach is to simulate a large array of counters using a cache mechanism 144" (¶ [0088]).

7. McFarling discloses "a serial branch predictor that includes a first component predictor operating according to a first algorithm to predict an action, and any number of subsequent components predictors operating according to alternate algorithms to predict the action" (¶ [0030]).

8. McFarling discloses in FIG. **6**, "two independent predictors **60**, **62** operating in parallel" (¶ [0029]).

9. McFarling discloses that "the appropriate tag is set to correspond to the V^{30} value, and the counter **146** is initialized to weakly agree with the branch causing the miss" (¶ [0089]).

Yeh

10. Yeh discloses that "[w]hen the information encoded in an instruction indicates that there is a likely taken or likely not taken prediction, the compiler is not very sure whether the branch should be taken or not taken. In this case, BPT **140** is used for dynamically predicting the behavior of branches" (col. 6, ll. 19-23).

11. Yeh discloses that "the microprocessor may use the taken/not-taken field of the two-bit compiler hint to determine whether a branch should be taken or not taken" (col. 6, ll. 32-34).

IV. PRINCIPLES OF LAW

Appellants have the burden on appeal to the Board to demonstrate error in the Examiner's position. See *In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006) ("On appeal to the Board, an applicant can overcome a rejection [under § 103] by showing insufficient evidence of *prima facie* obviousness or by rebutting the *prima facie* case with evidence of secondary indicia of nonobviousness.") (quoting *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998)). Therefore, we look to Appellants' Brief to show error in the proffered prima facie case. Only those arguments actually made by

Appellants have been considered in this decision. Arguments which Appellants could have made but chose not to make in the Brief has not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii).

V. ANALYSIS

Grouping of Claims

In the Brief:

Group I: Appellants essentially argue claims 1, 3, 4, 6, 13, 14, 16, 17, 19, 26, and 27 as a group (App. Br. 6-12). For claims 3, 4, 6, 13, 14, 16, 17, 19, 26, and 27, Appellants repeat the same argument made for claim 1. We will, therefore, treat claims 3, 4, 6, 13, 14, 16, 17, 19, 26, and 27 as standing or falling with claim 1.

Group II: Appellants argue claims 2, 7, 8, 15, 20, and 21 as a group (App. Br. 12-13). For claims 7, 8, 15, 20, and 21, Appellants repeat the same argument made for claim 2. We will, therefore, treat claims 7, 8, 15, 20, and 21 as standing or falling with claim 2.

Group III: Appellants argue claims 9-11 and 22-24 as a group (App. Br. 14-15). For claims 10, 11, and 22-24, Appellants repeat the same argument made for claim 9. We will, therefore, treat claims 10, 11, and 22-24 as standing or falling with claim 9.

See 37 C.F.R. § 41.37(c)(1)(vii). *See also In re Young,* 927 F.2d 588, 590 (Fed. Cir. 1991).

The Obviousness Rejection

We now consider the Examiner's rejection of the claims under 35 U.S.C. § 103(a).

Group I
Claims 1, 3, 4, 6, 13, 14, 16, 17, 19, 26, and 27

Appellants contend that "Loh does not teach[,] disclose[,] or suggest that the branch predictor units 405 have any storage capacity whatsoever" (App. Br. 8). Appellants further contend that "the branch history information is stored in the prediction history registers 401 and not the branch predictor 405" (*Id.*).

The Examiner found that Appellants' contentions "appears to be admission by the Appellant[s] that there is a first and second storage that stores prediction information" (Ans. 12).

Issue: Have Appellants shown that the Examiner erred in finding that the Loh admittedly discloses first and second storages, including a plurality of locations for storing first and second sets of partial prediction information?

While Appellants argue that Loh's branch prediction units 405 do not have any storage capacity whatsoever, Appellants expressly state that Loh discloses prediction history registers 401 for storing such branch history (App. Br. 8). The Examiner finds that such a statement by the Appellants

amounts to a clear admission that Loh discloses first and second storages that store prediction information (Ans. 12). We agree.

For example, Loh specifically discloses that the prediction history register 401 stores prediction history and that such a register may also be memory location within the processor (FF 1). Thus, given the aforementioned disclosure of Loh and Appellants' above noted admission, we find that the claimed first and second storage including a plurality of locations for storing prediction information reads on Loh's storage of prediction history in the prediction history register 401 and/or memory locations. In Loh's register 40, information may be accessed in segments, i.e., segment 1, segment 2, etc., by a number of intermediate branch prediction units 405 (Loh, Fig. 4). Thus, we find that the claimed first/second storage including first/second plurality of locations for storing first/second sets of information reads on Loh's register 401 segments.

Appellants further contend that "it appears McFarling is using two hash functions (XOR) to access a single cache structure 144. In addition, Appellant notes the second hash function is operating on at least a portion of the result from the first hash function. This is in contrast to the assertions made by the Examiner, and to Appellant's recited claim language" (App. Br. 11).

The Examiner found that "McFarling discloses utilizing a hashing function to index global predictors" (Ans. 5). The Examiner further found that "McFarling is used to teach the obviousness of using hashing functions

and that it is unreasonable to believe the McFarling and Loh can be combined without adaptations [sic]. Loh teaches multiple cache structures that can be utilized . . ." (Ans. 13).

Issue: Have Appellants shown that the Examiner erred in finding that the combination of Loh and McFarling discloses performing first and second hash functions on input branch information to generate first/second indexes for accessing a selected location within said first/second storage?

As noted *supra,* the Examiner relies on Loh to disclose multiple cache locations. The Examiner however relies on McFarling to disclose the feature relating to performing hash functions on input branch information to generate indexes for accessing storage locations (Ans. 13). For example, McFarling discloses a gshare predictor scheme that uses branch instruction address to index the array of counters whereby the hashing allows using more history bits and more address bits (FF 4-5). McFarling further discloses that the index value V could be used to directly access an array of counters in a cache (FF 6). In other words, while Loh disclose multiple cache locations, McFarling discloses performing multiple hash functions to generate indexes for accessing cache locations. Thus, we find that the combination of Loh and McFarling reasonably suggests performing first/second hash functions on input branch information to generate first/second indexes for accessing locations within first/second storages.

In addition, McFarling further discloses a scheme whereby a *serial* branch predictor is used and a scheme whereby two independent predictors

operate in *parallel* (FF 7-8). Similarly, Loh discloses that some of its intermediate branch history units may be in parallel and others may be in series (FF 2). Thus, we further find that both Loh and McFarling contemplate using parallel and series configurations in their prediction schemes.

In other words, McFarling discloses hash functions that can operate serially, i.e., subsequent stages focusing on correcting predictions made by a prior stage, and hash functions that operate independently in parallel. While we agree with Appellants that McFarling discloses a second hash function that operates on at least a portion of the result from the first hash function e.g., serial operation, Appellants have not shown how this is distinguishable from the claimed first and second hash functions. For example, while claim 1 requires performing first and second hash functions on input branch information, claim 1 does not require that such hash functions are independent of each other. For instance, McFarling discloses stages of hash functions being performed on the input branch information (e.g., in the serial application). Furthermore, McFarling also discloses a parallel application whereby a first hash function (e.g., bimodal or local) and second hash function (e.g., global) are perform independently on the input branch information (McFarling, Fig. 6). Thus, we find that the claimed first and second hash function reads on both McFarling's serial and parallel hash functions.

As to the other recited elements of claim 1, Appellants provide no argument to dispute that the Examiner has correctly shown where all these claimed elements appear in the prior art. Thus, we deem those arguments waived. *See* 37 C.F.R. § 41.37(c)(1)(vii) (2004).

We find that the Examiner has set forth a sufficient initial showing of obviousness, and we find that Appellants have *not* shown error in the Examiner's rejection of illustrative claim 1. Therefore, we affirm the rejection of independent claim 1 and of claims 3, 4, 6, 13, 14, 16, 17, 19, 26, and 27, which fall therewith.

Group II
Claims 2, 7, 8, 15, 20, and 21

Appellants contend that "Loh ONLY teaches 'a final branch history predictor unit 410 to generate a final branch prediction as function of the intermediate branch performed by the intermediate predictions branch prediction units.' Loh is silent as to how this is performed. The Examiner is merely speculating that Loh teaches how the predictions are performed" (App. Br. 12).

The Examiner found that Loh discloses the features of claim 2 at paragraphs [0020-0022] and that "the use of strength in branch prediction is well known" (Ans. 14).

Issue: Have Appellants shown that the Examiner erred in finding that it was well known that prediction values indicate of how strongly/weakly taken/not taken a prediction value is?

While we agree with Appellants that paragraphs [0020-[0022] of Loh discloses a final branch prediction based off of the intermediate branch prediction (FF 3), McFarling discloses that the prediction value may correspond to a tag indicating how weak the branch miss may be (FF 9). Thus, we find that the Examiner has established that the use of strength in prediction values was well known at the time of the invention.

Regarding the "summing" feature in claim 8, Appellants contend that there is no teaching of this feature in Loh. However, the Examiner relies upon McFarling to teach/suggest such a feature (Ans. 8: Ans. 15). Appellants have not provided any arguments to dispute the Examiner's findings. Thus, we summarily affirm this rejection.

As such, we find that the Examiner has set forth a sufficient initial showing of obviousness, and we find that Appellants have not shown error in the Examiner's rejection of claim 2. Therefore, we affirm the rejection of claim 2, and of claims 7, 8, 15, 20, and 21 which falls therewith.

Group III
Claims 9-11 and 22-24

Appellants contend that "Yeh is teaching using the HW branch predictor if the hint confidence is not strong enough. This is not the same as 'a plurality of counter values each corresponding to a strongly/weakly agree/disagree indication that is indicative of whether said branch prediction

hint bit embedded within said current branch instruction is to be used by said control unit'" (App. Br. 15).

The Examiner found that "Yeh discloses using a hardware branch predictor if confidence in the compiler hint is not strong, that is, if the compiler is below a threshold of assuredness a branch prediction is further utilized to determine whether the hint bit is correct" (Ans. 9).

Issue: Have Appellants shown that the Examiner erred in finding that Yeh discloses whether a branch prediction is performed in accordance with a branch prediction hint encoded within the current branch instruction?

Yeh discloses that information encoded in an instruction, i.e., the two-bit taken/not taken field of the compiler hint, can be used to determine whether a branch should be taken or not (FF 10-11). Claim 9 recites *". . . use said prediction value to control whether a branch prediction is performed in accordance with a branch prediction hint encoded within the current branch instruction."* (Emphasis added). Appellants have not shown how the prediction hint feature of claim 9 is distinguishable from Yeh's compiler hint feature. Appellants merely assert that they are not the same without providing any meaningful analysis as to why. For example, both systems start with a prediction value and makes further determination based on a prediction hint. Thus, we find that the aforementioned claim limitation reads on Yeh's microprocessor using the compiler hint to determine whether a branch should be taken or not.

In addition, Appellants assert that they disagree "that it would be obvious to generate 'said prediction value . . . by summing respective counter values" (App. Br. 15). However, again Appellants merely argue that they disagree with the Examiner's findings without providing any meaningful analysis that explains why the Examiner erred. A statement which merely points out what a claim recites will not be considered an argument for separate patentability of the claim. *See* 37 C.F.R. § 41.37(c)(1)(vii). We note that arguments which Appellants could have made but chose not to make in the Briefs have not been considered and are deemed to be waived.

As such, we find that the Examiner has set forth a sufficient initial showing of obviousness, and we find that Appellants have *not* shown error in the Examiner's rejection of claim 9. Therefore, we affirm the rejection of claim 9, and of claims 10, 11, and 22-24 which falls therewith.

VI. CONCLUSIONS

We conclude that Appellants have *not* shown that the Examiner erred in rejecting claims 1-4, 6-11, 13-17, 19-24, 26, and 27.

VII. DECISION

In view of the foregoing discussion,

We affirm the Examiner's rejection of claims 1-4, 6-11, 13-17, 19-24, 26, and 27.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a). *See* 37 C.F.R. § 1.136(a)(1)(iv) (2007).

AFFIRMED

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